

CURRICULUM VITAE

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EMPLOYMENT

The University of Arizona, Tucson <i>Professor of Electrical Engineering and Mathematics</i> <i>da Vinci Circle Fellow</i> <i>Director of Error Correction Laboratory</i>	2000–present
Bell Laboratories <i>Member of Technical Staff</i>	1998–2000
Kodak Research Laboratories <i>Senior Research Scientist</i>	1997–1998
Rochester Institute of Technology <i>Research Fellow</i>	1996–1997
University of Nis, Serbia <i>Assistant Professor</i>	1994–1996

EDUCATION

University of Nis, Serbia <i>Ph.D. in Electrical Engineering</i> The youngest Ph.D. at University of Nis, School of Engineering	1994
University of Nis, Serbia <i>MS in Electrical Engineering</i>	1991
University of Nis, Serbia <i>Dipl.-Ing. in Electrical Engineering</i> Award for a student with the largest GPA at the University Serbian Academy of Science and Arts (SANU) Scholarship	1989

HONORS AND DISTINCTIONS

<i>NASA SURP</i>	2022
<i>IEEE Fellow</i> “For contributions to coding theory and its application in data storage systems and optical communications”	2013
<i>Fulbright Scholar</i>	2015
<i>Kenneth Von Behren Chair</i>	2012
<i>da Vinci Fellow</i>	2012
<i>IEEE International Conference on Quantum Computing and Engineering (QCE)</i> <i>Algorithms Category Best Paper Award</i>	2024
<i>IEEE Data Storage Paper Award</i>	2009
<i>Institute of Advanced Study Grant</i> Université Paris-Seine	2018
<i>IEEE Communication Theory Workshop Best Poster Award</i>	2014
<i>Best of Show Award for the Most Innovative Flash Memory Technology – Codelucida</i> Flash Memory Summit	2019

<i>I-Squared Startup of the Year for Codelucida</i> Tech Launch Arizona	2018
<i>Institute of Advanced Study Grant</i> Université Paris Seine	2018
<i>Expert Panel Chair</i> Flash Memory Summit	2016–2018
<i>Arizona Innovation Challenge Award for Codelucida</i> Arizona Commerce Authority	2017

RESEARCH HIGHLIGHTS

Error Correction Laboratory: Coding theory and applications to quantum computing, optical communications, flash memories, cloud storage, and wireless communications. A co-PI on two Quantum Centers responsible for developing quantum error correction systems for quantum internet (NSF), and for superconducting systems (DoE, Fermilab). PI or co-PI on seven additional NSF grants, and NASA-SURP grant.

Fermi National Accelerator Laboratory: Quantum Error Correction Team Lead in the Superconducting Materials and Systems Center funded by Department of Energy and led by Fermi National Accelerator Laboratory.

Bell Labs: An inventor of the soft error-event decoding algorithm, and the key architect of a detector/decoder for Bell Labs data storage read channel chips which were regarded as the best in industry. Different variants of this algorithm were implemented in virtually all magnetic hard drives.

LDPC Codes: Pioneering work on structured low-density parity check (LDPC) error correcting codes and iterative decoders. Designed of codes and decoders with best error-floor performance known today. Structured LDPC codes are a coding scheme of choice in almost all communication system standards, including WiFi.

Codelucida: Founder and Chief Scientific Officer of Codelucida, a company founded in 2012, developing error correction coding solutions for solid state drives used in data centers.

RECENT FUNDED RESEARCH HISTORY

NSF ERC (co-PI, share – %) <i>Center for Quantum Networks</i>	\$50,520,000,000 2020–2030
DoE Fermilab (co-PI, share – %) <i>Superconducting Quantum Materials and Systems Center</i>	\$115,000,000 2020–2025
NSF CIF (PI, share – 50%) <i>Quantum LDPC Codes and Low-Complexity Iterative Decoders</i>	\$600,000 2025–2028
NASA SURP (PI, share – 100%) <i>Robust Neural Network Decoders for Quantum Error Correction Systems</i>	\$80,000 2021–2024
NSF CIF (PI, share – 50%) <i>Learning To Correct Errors</i>	\$491,424 2021–2025
NSF CCSS (PI, share – 50%) <i>Secure and Efficient Post-quantum Cryptography</i>	\$245,000 2021–2025
NSF CIF-Medium (PI, share – 50%) <i>QODED: Quantum codes Optimized for the Dynamics between Encoded Computation and Decoding using Classical Coding Techniques</i>	\$699,076 2021–2025
NSF CIF-Medium (PI, share – 50%) <i>QODED: BPC Pilot Supplement</i>	\$139,797 2022–2025
NSF ECCS/CCSS (PI, share – 100%) <i>Neural Network Nonlinear Iterative LDPC Decoders with Guaranteed Error Performance and Fast Convergence</i>	\$320,000 2020–2025
NSF CIF (PI, share – 70%) <i>Iterative Quantum LDPC Decoders</i>	\$1,125,487 2019–2024

INTERNATIONAL RESEARCH COLLABORATION

Quanterra <i>EQUIP (Error correction for QUantum Information Processing)</i>	\$2,000,000 2022–2025
NSF <i>CoQREATE (US-Ireland Collaboration, Center for Quantum Networks)</i>	\$90,000 2023–2025
Agence Nationale de la Recherche ANR <i>NAND - Noise Against Noise Decoders</i>	\$2,000,000 2016–2019
European Commission FET-FP7 <i>FET-OPEN Innovative Reliable Chip Designs from Low-Powered Unreliable Components (i-RISC) (FET program success rate 1-2%)</i>	\$2,445,272 2013–2016
European Commission FP7 <i>Media Pipe - Error Correction Codes for Multimedia Communications</i>	\$5,000,000 2004–2006
Indo-US Technology Forum JC-16-2014-US <i>Joint Networked Center for Data Storage Research (Indian Institute of Science University of Arizona, UCSD and Georgia Tech)</i>	\$70,000 2016–2018

RECENT CONFERENCE ORGANIZATION

Information Theory Workshop (ITW 2026) , Phoenix, Arizona, USA, <i>General Co-Chair</i>	2026
IEEE Quantum Week), Albuquerque, NM, USA <i>co-Organizer Quantum Error Correction: Pathways to Scalability Workshop</i>	2025
Schloss Dagstuhl , Leibniz Center for Informatics, Waden, Germany <i>co-Organizer Seminar on Error Correcting Codes: from Classical to Quantum</i>	2024
QuIK 2024 Workshop , Inaugural Quantum Information Knowledge Workshop, Athens, Greece <i>co-Creator, co-Organizer</i>	2024
IEEE Information Theory Workshop (ITW 2026) , Phoenix, Arizona <i>General co-Chair</i>	present
12th International Symposium on Topics in Coding (ISTC 2023) , Brest, France <i>Technical Program Chair</i> <i>Session co-Organizer, Quantum Error Correction: The Coding Theory Perspective</i> <i>Session co-Organizer - Quantum Error Correction: The Quantum Physics Perspective</i>	2023
11-th International Symposium on Topics in Coding (ISTC 2022) , Montreal, Canada, <i>Workshop Organizer and Technical Program Chair</i>	2022

PROFESSIONAL ACTIVITIES

PROFESSIONAL SOCIETIES

IEEE Information Theory Society <i>Co-Editor, Journal of Selected Areas in Information Theory (JSAIT)</i> <i>Special Issue on Quantum Error Correction and Fault Tolerance</i>	2024-2025
Quantum Economic Development Consortium (QED-C) <i>Member, Workforce Technical Advisory Committee</i>	2019-2022
IEEE Communications Society <i>Chair, Data Storage Technical Committee</i>	2015-2016

IEEE Communications Society <i>Chair, Tucson Joint AP/MTT/EMC/COMM Chapter</i>	2011-2019
IEEE Communications Society <i>Chair, Data Storage Technical Committee Best Paper Award</i>	2015-2016
IEEE Society <i>Student Member, Member, Senior Member, Fellow</i>	2018-present
IEEE Communications Society <i>Member, Communication Theory Technical Committee</i>	2001-present
IEEE Communications Society <i>Member, IEEE Data Storage Technical Committee</i>	2001-present
IEEE Standardization Association <i>Member, IEEE Working Group on Error Correction Coding for Non-Volatile Memories</i>	2013-2015

SELECTED RECENT AND INFLUENTIAL PUBLICATIONS

A list of recent publications can be found [here](#).

- [1] Q. Xu, J. P. B. Ataiades, C. A. Pattison, N. Raveendran, D. Bluvstein, J. Wurtz, B. Vasić, M. D. Lukin, L. Jiang, and H. Zhou, “Constant-overhead fault-tolerant quantum computation with reconfigurable atom arrays,” *Nature Physics*, pp. 1084—1090, April 2024. [Online]. Available: <https://doi.org/10.1038/s41567-024-02479-z>
- [2] S. K. Borah, A. K. Pradhan, N. Raveendran, N. Rengaswamy, and B. Vasić, “Non-binary hypergraph product codes for qudit error correction (Best Paper Award),” in *2024 IEEE International Conference on Quantum Computing and Engineering*, Sept. 2024, pp. 1–11. [Online]. Available: <https://arxiv.org/abs/2406.17070>
- [3] N. Raveendran and B. Vasić, “Trapping Sets of Quantum LDPC Codes,” *Quantum*, vol. 5, p. 562, Oct. 2021. [Online]. Available: <https://doi.org/10.22331/q-2021-10-14-562>
- [4] S. S. Garani and B. Vasić, “Channels engineering in magnetic recording: From theory to practice,” *IEEE BITS, the Information Theory Magazine*, vol. 2, no. 3, pp. 6–49, December 2024.
- [5] N. Raveendran, E. Boutillon, and B. Vasić, “Turbo-XZ algorithm: Low-latency decoders for quantum LDPC codes,” in *2023 IEEE International Symposium on Topics in Coding (ISTC)*, September 2023, pp. 1–5. [Online]. Available: <https://hal.science/hal-04203861v1/document>
- [6] N. Rengaswamy, N. Raveendran, A. Raina, and B. Vasić, “Entanglement purification with quantum LDPC codes and iterative decoding,” *Quantum*, vol. 8, 2024. [Online]. Available: <https://quantum-journal.org/papers/q-2024-01-24-1233/>
- [7] N. Raveendran, N. Rengaswamy, A. K. Pradhan, and B. Vasić, “Soft syndrome decoding of quantum LDPC codes to correct of data and syndrome errors,” in *2022 IEEE International Conference on Quantum Computing and Engineering (QCE)*, Sep. 2022, pp. 275–281. [Online]. Available: <https://arxiv.org/abs/2205.02341>
- [8] N. Raveendran, N. Rengaswamy, F. Rozpędek, A. Raina, L. Jiang, and B. Vasić, “Finite rate QLDPC-GKP coding scheme that surpasses the CSS Hamming bound,” *Quantum*, vol. 6, p. 767, 2022. [Online]. Available: <https://arxiv.org/abs/2111.07029>
- [9] S. Adiga, X. Xiao, R. Tandon, B. Vasić, and T. Bose, “Generalization bounds for Neural Belief Propagation decoders,” *IEEE Transactions on Information Theory*, vol. 70, no. 6, pp. 4280–4296, June 2024. [Online]. Available: <https://arxiv.org/abs/2305.10540>
- [10] X. Xiao, B. Vasić, R. Tandon, and S. Lin, “Designing finite alphabet iterative decoders via recurrent quantized neural networks,” *IEEE Transactions on Communications*, vol. 68, no. 7, pp. 3963–3974, Jan. 2020.
- [11] S. Brkic, P. Ivaniš, and B. Vasić, “Adaptive gradient descent bit-flipping diversity decoding,” *IEEE Communications Letters*, vol. 26, no. 10, pp. 2257–2261, Oct. 2022.

- [12] N. Raveendran, D. Declercq, and B. Vasić, “A sub-graph expansion-contraction method for error floor computation,” *IEEE Transactions on Communications*, vol. 68, no. 7, pp. 3984–3995, 2020.
- [13] S. Brkic, P. P. Ivaniš, and B. Vasić, “Majority logic decoding under data-dependent logic gate failures,” *IEEE Transactions on Information Theory*, vol. 63, no. 10, pp. 6295–6306, October. 2017.
- [14] B. Vasić and P. Ivanis, “Error errore eicitur: A stochastic resonance paradigm for reliable storage of information on unreliable media,” *IEEE Transactions on Communications*, vol. 64, no. 9, pp. 3596–3608, 2016.
- [15] E. Dupraz, D. Declercq, B. Vasić, and V. Savin, “Analysis and design of finite alphabet iterative decoders robust to faulty hardware,” *IEEE Transactions on Communications*, vol. 63, no. 8, pp. 2797–2809, Aug 2015.
- [16] D. V. Nguyen and B. Vasić, “Two-bit bit flipping algorithms for LDPC codes and collective error correction,” *IEEE Trans. Comm.*, vol. 62, no. 4, pp. 1153–1163, April 2014.
- [17] D. Declercq, B. Vasić, S. K. Planjery, and E. Li, “Finite alphabet iterative decoders, Part II: Improved guaranteed error correction of LDPC codes via iterative decoder diversity,” *IEEE Trans. Commun.*, vol. 61, no. 10, pp. 4046–4057, Nov. 2013.
- [18] S. K. Planjery, D. Declercq, L. Danjean, and B. Vasić, “Finite alphabet iterative decoders, Part I: Decoding beyond belief propagation on the binary symmetric channel,” *IEEE Trans. Commun.*, vol. 61, no. 10, pp. 4033–4045, Nov. 2013.
- [19] D. V. Nguyen, S. K. Chilappagari, B. Vasić, and M. W. Marcellin, “On the construction of structured LDPC codes free of small trapping sets,” *IEEE Transactions on Information Theory*, vol. 58, no. 4, pp. 2280–2302, Apr. 2012.
- [20] B. Vasić, D. Nguyen, and S. K. Chilappagari, *Chapter 6 - Failures and Error Floors of Iterative Decoders*. Oxford: Academic Press, 2014, pp. 299 – 341.
- [21] S. Chilappagari and B. Vasić, “Error-correction capability of column-weight-three LDPC codes,” *IEEE Transactions on Information Theory*, vol. 55, no. 5, pp. 2055–2061, May 2009.
- [22] S. K. Chilappagari, D. V. Nguyen, B. Vasić, and M. W. Marcellin, “On trapping sets and guaranteed error correction capability of LDPC codes and GLDPC codes,” *IEEE Transactions on Information Theory*, vol. 56, no. 4, pp. 1600–1611, April 2010.
- [23] —, “Error correction capability of column-weight-three LDPC codes under the Gallager a algorithm - Part II,” *IEEE Transactions on Information Theory*, vol. 56, no. 6, pp. 2626–2639, June 2010.
- [24] S. Chilappagari, D. V. Nguyen, B. Vasić, and M. Marcellin, “On trapping sets and guaranteed error correction capability of LDPC codes and GLDPC codes,” *IEEE Transactions on Information Theory*, vol. 56, no. 4, pp. 1600–1611, Apr. 2010.
- [25] D. V. Nguyen, S. Chilappagari, M. Marcellin, and B. Vasić, “On the construction of structured LDPC codes free of small trapping sets,” *IEEE Transactions on Information Theory*, vol. 58, no. 4, pp. 2280–2302, Apr. 2012.
- [26] B. Vasić and O. Milenkovic, “Combinatorial constructions of low-density parity-check codes for iterative decoding,” *IEEE Transactions on Information Theory*, vol. 50, no. 6, pp. 1156–1176, June 2004.
- [27] S. K. Chilappagari, M. Chertkov, and B. Vasić, “An efficient instanton search algorithm for LP decoding of LDPC codes over the BSC,” *IEEE Transactions on Information Theory*, vol. 57, no. 7, pp. 4417–4426, Jul. 2011.
- [28] M. Ivkovic, S. K. Chilappagari, and B. Vasić, “Eliminating trapping sets in low-density parity-check codes by using tanner graph covers,” *IEEE Transactions on Information Theory*, vol. 54, no. 8, pp. 3763–3768, 2008.
- [29] B. Vasić and S. K. Chilappagari, “An information theoretical framework for analysis and design of nanoscale fault-tolerant memories based on low-density parity-check codes,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 11, pp. 2438–2446, Nov. 2007.