Specification for the book of courses

Study program	Electrical Engineering and Computer Science		
Module	Electronics - Electronic Circuits and Embedded Systems		
Type and level of studies	Undergraduate Academic Studies		
The name of the course	Functional Verification		
Lecturer (for lectures)	Andrejević-Stošović V. Miona, Dimitrijević A. Marko		
Lecturer/associate (for exercises)			
Lecturer/associate (for OFE)	Andrejević-Stošović V. Miona, Dimitrijević A. Marko		
Number of ECTS	5	**Course status (obligatory/elective)**	Obligatory
Prerequisites			
Course objectives	Students need to adopt and systematize knowledge related to the functional verification of integrated circuits, from module-block verification to system verification.		
Course outcomes	Acquiring competences for functional verification at block level. Students gain competences to use software tools for verification (Specman), make a verification plan, define a verification environment, and verify a simple block or component.		
Course outline			
Theoretical teaching	Basics of Verilog language. The basic elements of the 'e' language. Paradigms of 'e' language - an object-oriented, declarative, aspect paradigm. Notion of time in Specman. Events - definition and usage. Ordinary and Time Consuming Methods. Inheritance - like / when. Basic concepts of Specman verification: organization and import of files, connecting verification environment with design, design simulation, execution steps, objects in the verification environment: driver, collector, checker. Advanced features of 'e': the characteristics of ports, pointers, messages and coverage. Block-level verification and system-level verification: verification environment for module and block level, verification environment for system level, verification strategy. Basics of 'e Reuse' methodology: eVC architecture, End-of-test methodology, Reset methodology, packaging and encapsulation, organization of source files.		
Practical teaching (exercises, OFE, study and research work)	Knowledge obtained in lectures students deepen by acquiring skills in realization of the verification environment using the professional tool Specman. 1. UNIX environment basics (text files) 2. Basics of Verilog language and simulations 3. 'e' language - data types, structures, units, methods, events ... 4. Introduction to verification methodology 5. Verification of the FIFO block		
Textbooks/references			
1	S. Iman, S. Joshi, The e hardware verification language, Kluwer Academic Publishers, New York, 2004.		
2	David Robinson, Aspect-Oriented Programming with the e Verification Language, 1st Edition, Elsevier, ISBN: 9780123742100, 2007.		
3			
4			
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Number of classes of active education per week during semester/trimester/year				
Lectures	**Exercises**	**OFE**	**Study and research work**	**Other classes**
2	0	2	0	0
Teaching methods	Lectures, practical exercises and examples, projects			

Grade (maximum number of points 100)			
Pre-exam duties	**Points**	**Final exam**	**Points**
Activity during lectures	25	**Written exam**	
Exercises	25	**Oral exam**	50
Colloquia			
Projects			