Specification for the book of courses

Study program	Electrical Engineering and Computer Science		
Module	Electronics - Electronic Circuits and Embedded Systems		
Type and level of studies	Undergraduate Academic Studies		
The name of the course	Hardware Modeling Languages		
Lecturer (for lectures)	Andrejević-Stošović V. Miona		
Lecturer/associate (for exercises)	Mirković D. Dejan		
Lecturer/associate (for OFE)	Mirković D. Dejan		
Number of ECTS	5	**Course status (obligatory/elective)**	Elective
Prerequisites			
Course objectives	Introducing the hardware description languages (HDL) used in designing and verifying integrated circuits: System Verilog, Verilog-AMS.		
Course outcomes	Accomplishing of competences for modeling of digital and analog electronic circuits using HDL languages. Students are expected to learn to correctly describe an electronic circuit according to the given specifications and confirm the functionality of the model with appropriate simulations. Students should learn how to write and present the results of the work.		
Course outline			
Theoretical teaching	Verilog as HDL. Bottom-up and Top-Down methodology. Module as a basic unit. Sequential Verilog. Operators. Registers. Memories. Statements for flow control. Loops. Subprograms. Concurrent processes. Blocking and Non-blocking assignment. Instances. Pins. Time in Verilog. Parameters. Directives. Testbenches. Basics of Verilog-AMS language for modeling and verifying analog blocks in a digital environment. Description of conservative (Kirchhoff laws) and non-conservative (signal flow) systems. Branches, nodes, signals. Functions of Verilog-A language for the implementation of basic analog functions. Examples of AMS models of analog blocks. Trade between the complexity of the AMS model and the simulation time.		
Practical teaching (exercises, OFE, study and research	Students improve their knowledge obtained in lectures by developing skills for writing and validating the Verilog model using compilers and simulators from the professional Cadence and Mentor Graphics software packages.		
Textbooks/references			
1	Sutherland, S., et al., SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling, 2013. ISBN 1475766823, 9781475766820		
2	Writing testbenches using SystemVerilog. Springer Science & Business Media, 2007. ISBN 1475766823, 9781475766820.		
3	IEEE Standard for SystemVerilog-Unified Hardware Design, Specification, and Verification Language," in IEEE Std 1800-2017 (Revision of IEEE Std 1800-2012) , vol., no., pp.1-1315, 22 Feb. 2018 doi: 10.1109/IEEESTD.2018.8299595		
4	Kundert, Ken, and Olaf Zinke. The designer's guide to Verilog-AMS. Springer Science & Business Media, 2006. ISBN 140208045X, 9781402080456.		
5	Verilog-AMSLanguage Reference Manual, Version 2.4.0, Accellera Systems Initiative 2014.		

Number of classes of active education per week during semester/trimester/year

Lectures	**Exercises**	**OFE**	**Study and research work**	**Other classes**
2	1	1	0	0
Teaching methods	Lectures, Auditory exercises, practical exercises and examples, projects			

Grade (maximum number of points 100)

Pre-exam duties	**Points**	**Final exam**	**Points**
Activity during lectures	10	**Written exam**	
Exercises	20	**Oral exam**	30
Colloquia			
Projects	40		