Specification for the book of courses

Study program	Electrical Engineering and Computer Science		
Module	Electronics - Electronic Circuits and Embedded Systems		
Type and level of studies	Undergraduate Academic Studies		
The name of the course	Digital System Design		
Lecturer (for lectures)	Đorđević Lj. Goran		
Lecturer/associate (for exercises)	Stojanović Z. Igor		
Lecturer/associate (for OFE)	Jovanović D. Milica		
Number of ECTS	5	**Course status (obligatory/elective)**	Elective
Prerequisites	Архитектуре дигиталних система		
Course objectives	The course objective is to teach students with principles and techniques of digital system design at register transfer level (RTL) of abstraction including: RTL design methodology, building blocks of digital systems, and basics of high-level synthesis.		
Course outcomes	At the end of this course, students are expected to use techniques, skills and modern engineering tools for medium and large-scale digital systems design including: a) design datapath and control unit of digital systems according to a stated functional behavior, b) design various arithmetic circuits (combinational and sequential), c) map algorithms to digital hardware, and d) integrate existing digital system cores into larger, more complex design		
Course outline			
Theoretical teaching	RTL design: control/datapath model of digital system, datapath organization, control unit design techniques, ASM representation of algorithm, optimization of ASM diagram, VHDL description of RTL system. RTL design for low-power. Clocking methodologies and synchronization. High-Level Synthesis: data-flow graph and transformations; architecture synthesis (allocation, resource sharing, register sharing, bus sharing, pipelining, area and performance optimization), scheduling (time-constrained scheduling, resource constrained scheduling, heuristic scheduling algorithms). Introduction to system-on-chip design and IP core based design.		
Practical teaching (exercises, OFE, study and research	Four laboratory exercises will be assigned with focus on RTL design and using FPGA EDA tools: 1) design and optimization of datapath; 2) VHDL-based design of large-size standard digital components; 3) design and performance evaluation of various types of arithmetic circuits; 4) design and implementation of a simple RTL system according to a stated functional behavior. In addition, a larger RTL design project will be assigned as the course project.		
Textbooks/references			
1	P.P. Chu, „RTL Hardware Design Using VHDL, Coding for Efficiency, Portability, and Scalability“, John Wiley & Sons, Inc. Hoboken, New Jersey, 2006.		
2	D. Gajski, Principles of Digital Design, Prentice-Hall, Inc. Upper Saddle River, NJ, 1997.		
3	Digital system design - supplementary nodes, available at course web site.		
4			
5			

Number of classes of active education per week during semester/trimester/year				
Lectures	**Exercises**	**OFE**	**Study and research work**	**Other classes**
2	1	1	0	0
Teaching methods	Lectures, exercises, laboratory exercises, homework, consultations			

Grade (maximum number of points 100)			
Pre-exam duties	**Points**	**Final exam**	**Points**
Activity during lectures		**Written exam**	25
Exercises	30	**Oral exam**	25
Colloquia	20		
Projects			