Specification for the book of courses

Study program			Electronics and Microsystems	
Module			Electronics and Microsystems	
Type and level of studies			Master studies	
The name of the course			System on Chip	
Lecturer (for lectures)			Dimitrijević A. Marko, Andrejević-Stošović V. Miona	
Lecturer/associate (for exercises)				
Lecturer/associate (for OFE)			Dimitrijević A. Marko, Andrejević-Stošović V. Miona	
Number of ECTS	5	**Course status (obligatory/elective)**		Elective
Prerequisites				
Course objectives	Acquiring knowledge about basic characteristics, architecture and methods of system on chip design.			
Course outcomes	Mastering design of integrated circuits that contain all elements of an entire system. Students will learn the basic characteristics of the system on chip, design procedures, methods of solving fundamental and specific problems for the realization and production of such systems.			
Course outline				
Theoretical teaching	Modeling and specification of the system at a high level of abstraction. System performance analysis at an early stage of the design process. Analysis of the relationship between the hardware and software components of the system on chip, algorithms and architectures in order to optimize the system based on the requirements (specifications) and limitations. System on chip architectures (control, real-time systems, data processing). Hardware, software and interface synthesis. System simulation and verification, hardware/software (HW/SW) cosimulation. Network-on-chip. Examples of high-level applications and development environments for system on chip implementation (Chisel, Magma). Reuse of blocks, codesign.			
Practical teaching (exercises, OFE, study and research work)	The methodology and design tools at the system level. HW/ W co-design: analysis, partitioning, real-time operation, hardware acceleration. Virtual platform models, cosimulation, system prototyping on FPGA. Transaction-Level Modeling (TLM), SystemC, SystemVerilog, Electronic System-Level (ESL) languages. High-Level Synthesis (HLS): allocation, scheduling, binding, resource sharing. Integration of the system on the chip, verification and testing. The system on chip design using Chisel tools, realization of the prototype on the FPGA platform.			
Textbooks/references				
1	D. Black, J. Donovan, SystemC: From the Ground Up, Springer, 2004			
2	M. Zwolinski, Digital System Design with SystemVerilog			
3	M. J. Flynn, W. Luk, Computer System Design: System-on-Chip, Wiley, 2011			
4				
5				

Number of classes of active education per week during semester/trimester/year				
Lectures	**Exercises**	**OFE**	**Study and research work**	**Other classes**
2	0	2		
Teaching methods	Lectures, laboratory work, consultations, projects			

Grade (maximum number of points 100)			
Pre-exam duties	**Points**	**Final exam**	**Points**
Activity during lectures	25	**Written exam**	
Exercises	25	**Oral exam**	50
Colloquia			
Projects			