**PRESS RELEASE**

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# European project aims at providing innovative solutions allowing reliable circuits to be designed from low-powered unreliable components

The University of Nis, Faculty of Electronic Engineering, is a member of the consortium that will realize the FP7 project "Innovative Reliable Chip Designs from Low-Powered Unreliable Components (i-RISC)". This is small or medium-scale focused research project (STREP), submitted under the ICT FET Call FP7-ICT-2011-C. The negotation meeting will be held on September 19, 2012 in Brussels. The project start will expected to be January 1st, and its duration will be 36 months.

The i-RISC project brings together the outstanding knowledge and expertise of the six academic partners with established track records, both individually and collectively, which enables the consortium to cover all of the aspects of this research in a most favourable way: **Commissariat à l'Energie Atomique** (CEA, France, project coordinator), **University College Cork**, (UCC, Ireland), **Ecole Nationale Supérieure de l'Electronique et de ses Applications** (ENSEA, France), **Technische Universiteit Delft** (TUD, The Netherlands), **Universitatea Politehnica Timisoara** (UPT, Romania), and **University of Nis**, **Faculty of Electronic Engineering** (ELFAK, Serbia).

One of the most critical challenges for the next-generation electronic circuit design is the nanoscale integration of chips built of unreliable components. The ineluctable integration density increase and the imperative requirements of low-energy consumption, for energy preservation, can only be sustained through low-powered components, which will be inherently unreliable. The design of storage, interconnect, and processing elements will require completely new approaches, which are inconceivable without the use of powerful fault tolerant techniques.

The i-RISC project builds upon techniques from the sparse graph codes theory, graph based multi-objective optimization, and logic synthesis. It targets the design of effective error correcting codes and encoder/decoder architectures able to provide reliable error protection even if they themselves operate on unreliable hardware. The envisaged fault-tolerant codec will contribute to the reliable storage and transfer of digital information throughout the chip. i-RISC will also develop a specific method to embed the codec into the structural description of the circuit logical functionality, such that reliable data processing is achieved. The proposed solution will be assessed and validated based on accurate error models and energy measurement tools developed within the project.

Based on the i-RISC alignment with the target outcomes of the European Commission Work Programme, the project will provide strong and direct contributions to key areas that will improve the competitiveness of European academic research and industry in future ICT developments. In the forthcoming challenge of nanoscale technologies, the i-RISC project is an essential prerequisite for convincing the European industry about the added value and feasibility of this new design approach.

The motivited PhD students and postodocs in the field of Telecommunications are invited to be involved in the project realization at the Faculty of Electronic Engineering. The interested students can submit their CVs on adress: goran@elfak.ni.ac.rs.

## Press contacts


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